Application No.: 09/847391 Docket No.: MWS-069

REMARKS

Claims 1-33 were presented for examination. Claims 1-33 were rejected under 35 U.S.C. §102(e) as being anticipated by US Patent No. 6,618,839 to Beardslee et al. ("Beardslee"). Upon entry of this amendment, claims 1, 2, 3, 6, 7, 13-16, 17, and 19-26 are amended to include the "model" limitation. No new matter is added. Applicants respectfully request entry of the amendments under MPEP 714.12. The amendments do not require a new search of prior art upon its merits because the added "model" limitation was presented in some of the originally filed claims. Applicants respectfully submit that the amendments clarify the claimed invention by making clear that the finite state machine is in a model.

Beardslee discusses a method and system for providing enhanced debugging capabilities for fabricated hardware designs at a Hardware Description Language (HDL) level. Generic configurable trigger detection circuits were discussed for various specific situations. Examples of these specific situations includes state based Finite State Machines (FSMs), transition based FSMs, data-path registers, and temporal logic. Specialized design control circuitry were discusses to provide more efficient hardware.

Applicants respectfully submit that Beardslee fails to teach each and every element of the claimed invention. Applicants submit that Beardslee does not disclose a description of a finite state machine model, the description including a temporal logic operator for defining a temporal logic condition, as recited in independent claims 1, 16, and 19-27. In the claimed invention, users are able to describe a finite state machine model using a temporal logic operator. In other words, the temporal logic operator is incorporated into the description of the finite state machine model for defined the temporal logic condition in the claimed invention. The Examiner suggested that Beardslee teaches the feature in col. 34, lines 1-4 and col. 36, lines 26-46. Applicants respectfully disagree.

The cited sections discuss the operation of a generic configurable trigger detection circuit, and a circuit that implements a temporal logic. Nowhere did the cited sections discuss the use of a temporal logic operator in a description of a finite state machine. Furthermore, Beardslee defined a finite state machine as an electronic system control structure (col 11, lines 25-26), whereas in the claimed invention, finite state machine is used to model the behavior of a system

having discrete states. Beardslee further describes generic configurable trigger detection circuits under specific situations, including state based FSMs, transition based FSMs, data-path registers, and temporal logic (col. 34, lines 26-32). Applicants respectfully submit that FSMs and temporal logic are discussed separately in two different specific situations in Beardslee, and Beardslee does not discuss the incorporation of temporal logic in a description of FSM.

Accordingly, Beardslee does not teach or suggest the element of "a description of a finite state machine model, the description including a temporal logic operator for defining a temporal logic condition" in independent claims 1, 16, and 19-27. Applicants respectfully request the Examiner to reconsider and withdraw the rejection of independent claims 1, 16, 19-27 and their corresponding dependent claims 2-15, 17-18, and 28-33.

Application No.: 09/847391 Docket No.: MWS-069

CONCLUSION

In view of the above amendment, applicant believes the pending application is in condition for allowance.

Applicant believes no fee is due with this statement. However, if a fee is due, please charge our Deposit Account No. 12-0080, under Order No. MWS-069 from which the undersigned is authorized to draw.

Dated: November 24, 2004

Respectfully submitted,

By _____

Kevin J. Canning
Registration No.: 35,470
LAHIVE & COCKFIELD, LLP
28 State Street
Boston, Massachusetts 02109
(617) 227-7400
(617) 742-4214 (Fax)
Attorney For Applicant